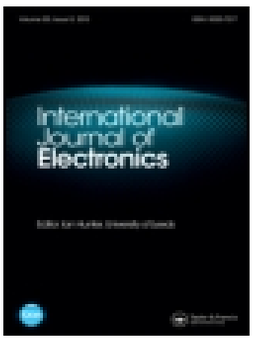

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Development of a 10-kV regional compensation dynamic voltage restorer with multiple functions

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ABSTRACT

The first 10-kV regional compensation dynamic voltage restorer (DVR) has been installed in a 110-kV substation in Shenzhen power grid, to protect plenty of sensitive loads in a wide area simultaneously from the disturbances caused by voltage sags. The location selection and performance indicators of the DVR are determined based on the voltage sag statistic results in recent years of Shenzhen power grid. The implementation schemes of main circuit elements, such as the energy storage unit, inverter and LC filter are presented. To further improve the DVR's cost-effectiveness, a novel virtual impedance control strategy is proposed to provide the DVR with a function of a Fault Current Limiter (FCL) or a Series Compensator (SC) besides the function of voltage sag compensation. Simulation and field experimental results are provided to show the correctness and effectiveness of the main circuit design and control system development of the 10-kV DVR.

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KEYWORDS
Dynamic voltage restorer (DVR); regional compensation; multiple functions; fault current limiter (FCL); virtual impedance control

I. Introduction

As a special economic zone and the fourth city in China, Shenzhen city has a huge volume of electric power consumption with a total electric load of over 10 million kilowatts. Shenzhen power grid is one of the most concentrated areas of high-tech industry worldwide and is characterised by a large number of large-scale industrial loads, which impose high press on the quality of the power supply. Comprehensive understanding of the present situation of the power quality, in-depth analysis of the demand of sensitive load on power supply quality, and cost-effective solutions for power quality problems have become some of the most important and urgent tasks of the power grids of large urban areas such as Shenzhen city.

At present, all substations of Shenzhen power grid have been covered by a power quality monitoring system that can provide five major categories of power quality indicators including system frequency deviation, three-phase voltage unbalance, voltage deviation, voltage flicker and harmonics. Statistics results of the records from 2012 to 2015 show that system frequency and three-phase voltage have a notably satisfying performance with basically 100% qualified rates, while voltage sags became the most prominent transient power quality problem due to the fact that its occurrence is far higher than those of voltage swells and short interruptions. For example, just in the year 2012, 2556 voltage sags events were recorded in 135 substations. In recent years, Shenzhen power grid has handled more than 21 complaints per year from large-scale customers on the production line outage or product scrap caused by the abnormality in power supply, and 70% of the complaints have been confirmed to originate from voltage sags. More seriously, the number of complaints showed an increasing yearly trend.

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Dynamic voltage restorer (DVR) has been recognised as the most effective measure against voltage sags problem because of its advantages such as fast response speed and high adaptability (Goharrizi, Hosseini, Sabahi, & Gharehpetian, 2012; Le, Wang, Yang, & Wang, 2018; Yan, Chen, Sun, Zhou, & Jiang, 2018; Zheng et al., 2018), which have been proven by the successful operation of several industrial equipment (e.g. (Gee, Robinson, & Yuan, 2017; Le, Wang, Yang, Zhang, & Li, 2018)). However, in China, the application of DVR is not yet popular mainly because of the argument between the owner of sensitive load and the power supply department regarding the investment of DVR. From the viewpoint of the former, power supply department has the responsibility to provide qualified power supply, and in turn, is certainly the investors of DVR. However, a mandatory standard about voltage sag governing has not been implemented in China at present, and it is unrealistic for power supply department to bear the huge investment solely in providing DVR for all sensitive users. Furthermore, this investment is hardly recovered through the so-called 'high price for high quality' scheme due to the lack of flexibility in electricity price constitution mechanism in China. Because of this dilemma, Shenzhen power grid has decided to perform a demonstration project for power quality comprehensive management, wherein a regional compensation 10-kV DVR is planned to develop and install in a 110-kV substation to simultaneously protect plenty of sensitive loads from voltage sags. This project aims to explore a road in satisfying the demand of all parties in voltage sag governing, and at the same time provide a theoretical basis and technical support to comprehensively improve the power quality of large urban power grids.

The remainder of this paper is structured as follows: In Section II, location selection and performance indices of the DVR are presented. Implementation of the main circuit and control system of the DVR is introduced in Section III and IV, respectively. Sections V and VI provide the simulation and field experimental results to show the correctness and effectiveness of the development of the DVR. The main findings are summarised in Section VII.

II. Location selection and performance indices

A. *Voltage sag statistics of Shenzhen power grid*

Figure 1 shows the statistics of voltage sag events of 10-kV distribution networks of Shenzhen power grid in 2010–2015.

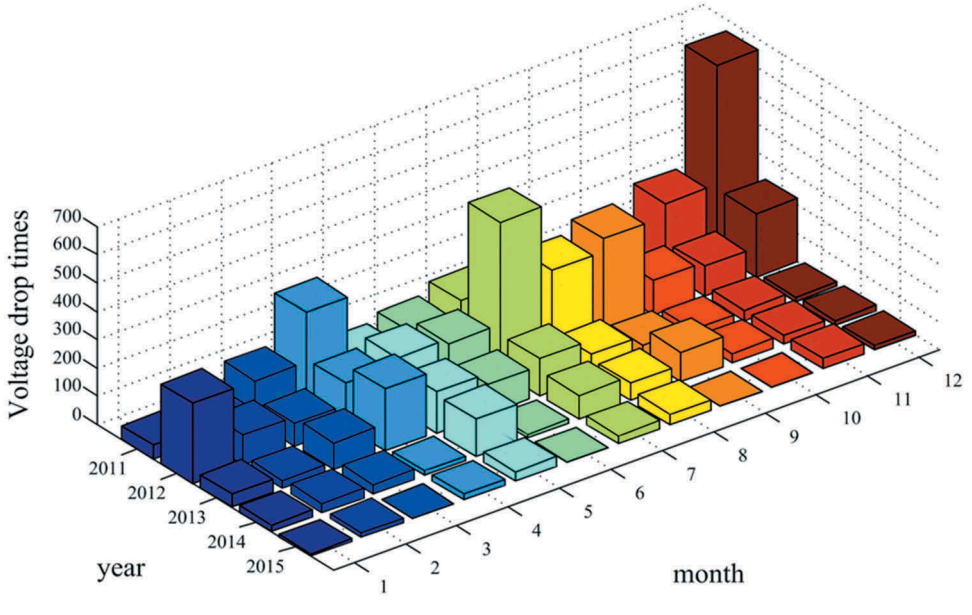


Figure 1. Statistics of voltage sag events in 10-kV networks.

From Figure 1 we can see that a total number of 6335 voltage sag events has been recorded during 2010–2015, implying that voltage sag is a notably prominent power quality problem in 10-kV networks of Shenzhen power grid, although some of these events may be recorded repeatedly by different monitoring devices. The most serious situation is in the year 2012 that there is a total number of 2556 events, and the number of voltage sags decreases gradually after 2012, mainly due to the efforts of Shenzhen power grid in governing voltage sag problem at the cost of massive manpower, materials and financial resources. Monthly statistic results show that the highest probability of voltage sag occurrence is from May to September every year, which well coincides with the climatic feature (thunderstorms) of Shenzhen as a coastal city.

B. *Install location selection*

According to the voltage sag statistics of all substations and the comprehensive considerations of several practical factors such as importance and concentration degree of sensitive loads, number of complaints about voltage sags and available space for DVR installation, a 110-kV substation is ultimately selected as the installation location. This substation has two 110-kV inlet lines, three 110/11-kV transformers with a rated capacity of 50MVA, four sections of 10-kV bus and 39 10-kV feeder lines. Figure 2 depicts the distribution of the recorded voltage sag event in #1 10-kV bus of this substation.

In choosing a feeder line for installation, we first bypass those without a backup supply to avoid a supply interruption associated with the required power outage during the installation of the device. Next, feeder lines supplying first-class loads that demand a notably high level of power supply reliability, and domestic loads that are normally insensitive to voltage sags, are totally ignored. Finally, feeder lines with a too large capacity of concentrated industrial load are excluded in considering the device capacity constraint. Table1 summarises the candidate feeder lines in the target substation and their basic information. Feeder line F07, which has a total distribution transformer capacity of 7.25-MVA and an average total load of 5.5-MVA, is the final winner to be protected by the DVR. Several semiconductor chip manufacturing enterprises are supplied by this feeder, and these enterprises have complained to the power supply department about the issue of voltage sags many times over the past years.

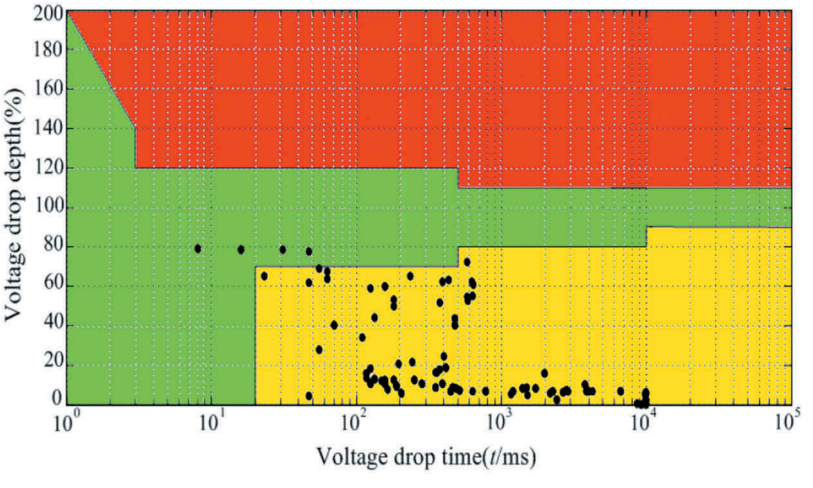


Figure 2. Voltage sag characteristics of the target substation.

Table 1. General information of the candidate feeder lines.

number	Load capacity (MVA)	Main load type	number	Load capacity (MVA)	Main load type
F01	3.872	I	F25	10	I
F03	7.5	C & D	F04	2.2572	C & D
F05	8.0	C & D	F06	1.9418	I & D
F07	5.51	I	F08	7.1706	D
F09	6.91	C	F10	6.346	C & D
F11	1.368	D	F12	8.8806	I & D
F13	3.5796	I & D	F18	3.3668	I
F15	4.1496	I	F22	5.9926	I & D
F21	5.951	C	F26	7.6	I

I: Industrial load; C: Commercial load; D: Domestic load.

Table 2. Performance index of the DVR.

number	Performance index	value
1	rated capacity	5MVA
2	Maximum compensation voltage: (single-phase)	0.5p.u.
3	Maximum compensation active power: single-phase/three-phase	1.67MW/3.5MW
4	Compensation duration time	1s
5	Response time	<5ms
6	Inverter rated DC voltage	5kV
7	DC voltage utilisation efficiency	0.8–1
8	Inverter efficiency	0.96

C. *Performance indices*

Considering the load capacity of Feeder line F07 and the characteristics of voltage sags such as the depth and duration shown in Figure 2, we determine several important performance indices of the DVR and list them in Table2. Technical risks and investment return also have been considered in this design process.

III. Main circuit elements design

Figure 3 shows the single-line diagram of the DVR system. The regional DVR is coupled into the feeder line through an LC filter, and its inverter consists of several cascaded single-phase full bridges, each of which is equipped with an uncontrollable rectifier. The multiple-secondary-winding transformer provides the energy needed for voltage sag compensation to the rectifiers from another 10 kV bus, which is powered by a 110/10-kV transformer different from the one that supplies Feeder line F07.

A. *Energy storage unit*

Energy storage unit, which provides the required energy for the DVR to compensate voltage sags and stabilise DC voltage of the inverter, can be categorised into two types: self-power (e.g. a capacitor bank with a large capacity, superconducting energy storage (De, Cipriano, Brandao, & Ramos, 2015; Somayajula & Crow, 2015), etc.) and external power (e.g. a controlled/uncontrolled rectifier powered by an external power grid) (Jimichi, Fujita, & Akagi, 2011). Considering the 5-MW capacity of this DVR, we prefer the external power scheme since that self-power scheme is unable to provide such a huge volume of electrical energy in a cost-effective manner.

As shown in Figure 3, the energy storage system of the DVR is mainly composed of a charging buffer circuit, a transformer with 18 secondary side windings (6 per phase and a total of 18 for three phases), a three-phase uncontrolled full-bridge rectifier and a DC capacitor bank. The charging buffer circuit comprises a charging current limiting resistor with a bypass switch. In the

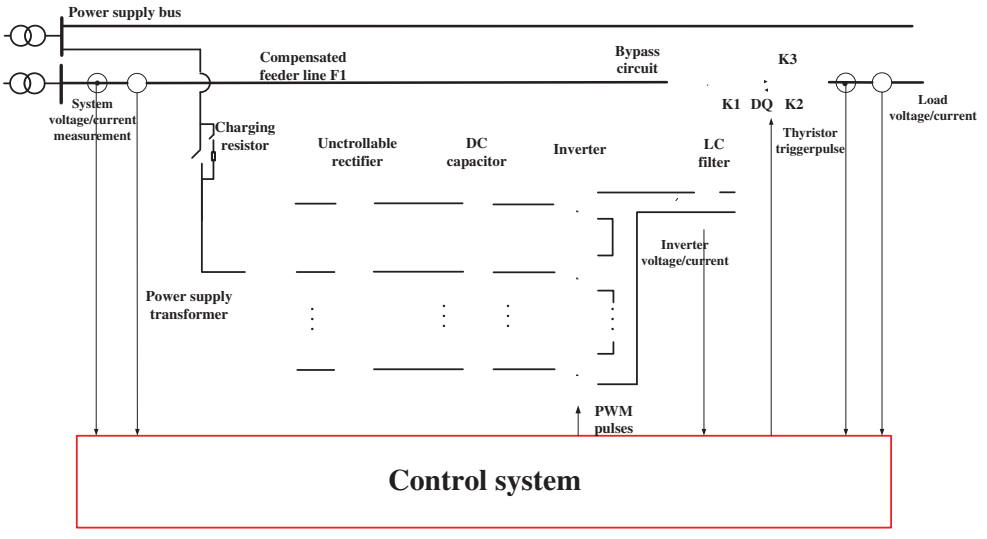


Figure 3. Single-line diagram of the DVR system.

energy charging process, the bypass switch is opened and the resistor is inserted into the circuit to limit the charging current impulse. After the DC voltage has reached its rated value, the bypass switch is closed to switch off the current-limiting resistor.

B. *Inverter*

The inverter of our DVR is structured by three independent single-phase full-bridges that can inject positive/negative/zero sequence voltages into feeder line conveniently and flexibly. Among current schemes for inverter in high-voltage scenario, the scheme that uses a transformer to step-up the voltage of an inverter has been gradually abandoned because of the high investment and large capacity of the transformer (Carlos, Jacobina, Santos, & Mello, 2018). Meanwhile, the degradation in voltage compensation due to the ferromagnetic nonlinear of the transformer is very hard to cope with even adopting advanced control strategies (Yin & Zhou, 2005). The scheme that power electronic devices connect in series and parallel only performs well for power electronic devices with a very high level of consistencies in their switching characteristics, thus it is rarely adopted in high-voltage equipment. Currently, multi-voltage-level schemes, especially the diode-clamped structure (Lv, Gao, Liu, & Chen, 2017) and the cascaded H-bridge structure (Shahabadini & Iman-Eini, 2016), are more appreciated by power electronic equipment with a large capacity and a high voltage level. The diode-clamped topology has been applied only to inverter with a voltage level of 5 or less. Therefore, we finally choose the cascaded H-bridge topology to develop the inverter of our DVR in view of its distinct advantages such as simple control, high scalability and no DC voltage sharing requirement.

As shown in Figure 3, each phase of the DVR inverter is composed of several H-bridges that connect in series with independent DC voltage supporting circuits, and each H-bridge is characterized by four 1700-V/1200-A IGBTs and a 1000-V DC voltage rating. The number N of the cascaded H-bridges can be determined in considering the maximum amplitude of the output voltage of each phase (0.5-p.u.) and the rated DC voltage (1-kV) of each phase inverter as:

$$(N-1)\times 1\,(\mathrm{kV}) < 0.5 \times 10\sqrt{2}/\sqrt{3} = 4.082\,(\mathrm{kV}) \le N \times 1\,(\mathrm{kV}) \tag{1}$$

The solution of formula (1) is $N = 5$, and we finally use six cascaded H-bridges in considering the system reliability.

C. *Output filter*

It is often advised to equip a cascaded H-bridge inverter with a low-pass output filter that is composed of a coupling capacitor and a filter inductor, as shown in Figure 3. In theory, the inductance of the filter should be of a sufficiently small value, on the one hand, to satisfy the requirement of fast current tracking, and on the other hand, should be sufficiently large to restrain the fluctuation in the output current of the inverter.

We can solve the lower value limit of the inductance in considering the situation that the inductor current is at its maximum value, that is:

$$L_{\min} = \frac{(NV_{\mathrm{dc}} - u_{\mathrm{cm}} \cos\varphi)[u_{\mathrm{cm}} \cos\varphi - (N-1)V_{\mathrm{dc}}]}{\Delta i_{\max} V_{\mathrm{dc}} f_{\mathrm{psw}}} \tag{2}$$

where N= 5 is the number of H-bridges in each phase; V_{dc} = 1000 V is the rated DC voltage of each H-bridge; u_{cm} = 0.5 p.u. and cosφ = 0.95 is, respectively, the maximum output voltage and power factor of the DVR; $f_{\mathrm{psw}} = 5 \times 1000$ Hz = 5000 Hz is the equivalent switching frequency of the inverter when the switching frequency of each H-bridge is 1000 Hz; $\Delta i_{\max}$ = 23 A is the maximum impulse current in the inductor that can be obtained from simulation results. In this project, L = 2500 μH is chosen finally.

The coupling capacitor can then be tuned by:

$$10 f_{\mathrm{n}} \leq f_{\mathrm{r}} = \frac{1}{2\pi\sqrt{LC}} \leq 0.1 f_{\mathrm{psw}} \tag{3}$$

where f_{n} = 50 Hz is the system fundamental frequency; f_{r} is the resonant frequency of the LC filter. We finally tune C = 20 μF for our DVR.

D. *By-pass circuit*

As shown in Figure 3, the by-pass circuit of the DVR is composed of an electronic bypass switch DQ, auxiliary dis-connectors K1 and K2 and a parallel mechanical switch K3. K3 is used to supply the load continuously when the DVR is out of service, and the electronic bypass switch is structured by a pair of anti-paralleling thyristors. In normal operation of the power grid (i.e. without voltage sags), DVR operates in a hot standby mode by opening K3 and closing DQ to bear the normal load current. Once detecting a voltage sag, DQ should be switched off as fast as possible to insert the output voltage of DVR into the protected feeder line. To forcefully and reliably turn-off the conducted thyristor in a very short period of time, we adopt a method that controlling the inverter to output a DC voltage which is normally larger than 100 V and has a polarity that is right reverse to the instantaneous direction of the current in the conducted thyristor. In this way, the requirement that the response time of the DVR is less than 5 ms is expected to be satisfied completely.

Special attention should be paid to short-circuit faults occurring downstream the DVR. In general, the right way in responding to this kind of fault is to close the mechanical bypass switch K3 and at the same time disconnect the DVR from the feeder line or a fault current with an amplitude up to dozens of kA is to flow through the electronic bypass switch DQ, threatening the security of the thyristor severely. However, this protection scheme may cause unnecessary frequent switching of the DVR especially for transient faults, and it is not always effective due to the relatively slow switching speed of the mechanical switch. In this paper, we propose a novel control strategy that employs the DVR to function as an FCL during the downstream faults. With the aid of this strategy, the problem of unnecessary frequent switching of the DVR can be tackled perfectly and the utilisation efficiency of

the DVR can be improved significantly. Most importantly, the mechanical bypass circuit, which is always the most vulnerable part of a DVR, is now can be omitted totally. The principle and implementation of the proposed strategy will be explained in the following section.

IV. Control system design

A. *Voltage sag compensation strategy*

At present, the most popular compensation strategies used by a DVR, such as in-phase voltage compensation (Sadigh & Smedley, 2012), complete voltage compensation (Jothibasu & Mishra, 2014) and minimum power compensation (Sun et al., 2010), are basically developed for DVRs in low-voltage (LV) distribution networks that operate in grounded neutral mode. While for middle-voltage (MV) network in China that operates in ungrounded neutral mode, zero-sequence component of the phase-to-neutral voltages cannot travel from an MV network to an LV one and vice versa. This finding implies that both the phase-to-phase and phase-to-neutral voltages of an LV network are acceptable as long as the phase-to-phase voltages in an MV network are acceptable, in other words, the zero-sequence component of the phase-to-neutral voltages of an MV network can be regulated by a DVR to optimise its compensation performance. We formally formulate this idea as:

$$\boldsymbol{U}_{j(dvr)} = \boldsymbol{U}_{j(\mathrm{com})} + \boldsymbol{U}_0 \quad j = a, b, c \tag{4}$$

where $\boldsymbol{U}_{j(\mathrm{dvr})}$ and $\boldsymbol{U}_{j(\mathrm{com})}$ is, respectively, the reference of the phase-to-neutral voltage of the DVR after and before optimisation, and $\boldsymbol{U}_{j(\mathrm{com})}$ can be obtained using, e.g. complete voltage compensation strategy; $\boldsymbol{U}_0$ is the zero-sequence voltage to be optimised by the DVR.

In this paper, we optimal $\boldsymbol{U}_0$ by considering: 1) the phase-to-neutral voltages at the load side of the DVR should not threaten the system insulation; 2) the output voltages of the DVR should not exceed 0.5p.u.; 3) increase symmetry degree of the output voltages of the DVR to maximise the use of the compensation ability of the DVR.

Without loss of generality, we take a three-phase asymmetrical voltage sag as the example to interpret the zero-sequence voltage optimisation method. The corresponding voltage phasors are shown in Figure 4.

In left graph of Figure 4, directed line segments OA′, OB′, OC′ and OA, OB, OC are the phasors of each system-side phase-to-neutral voltage before and after the compensation, respectively; $U_{a(\mathrm{com})}$,

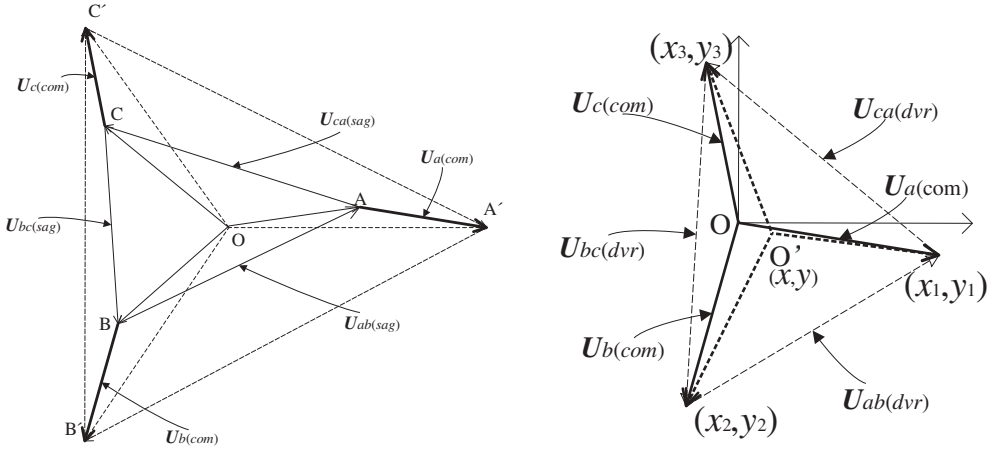


Figure 4. Voltage phasors in a three-phase asymmetrical voltage sag.

$U_{b(com)}$ and $U_{c(com)}$, which are represented by A'A, B'B and C'C, are the phasors of each phase reference voltage of the DVR that can be calculated using complete voltage compensation method (Jothibasu & Mishra, 2014). For the convenience of analysis, A'A, B'B and C'C are translated to be with the same starting point O. Achieving the optimisation goal while maintaining the phase-to-phase voltages $U_{ab(dvr)}$, $U_{bc(dvr)}$ and $U_{ca(dvr)}$ unchanged now can be transformed into the problem of finding a point O' in ΔA'B'C' that is of identical distances to the three vertices of this triangle.

From triangular geometry theory, we can know that O' exists and is unique such that: 1) if ΔA'B'C' is an acute triangle, then O' is the circumcenter of this triangle; and 2) if ΔA'B'C' is a right-angled or obtuse triangle, O' is the midpoint of the longest side of ΔA'B'C'. The directed line segment OO' is the phasor of the optimal zero sequence voltage $\boldsymbol{U}_{0opt}$.

B. *PWM strategy*

Multi-carrier modulation PWM (Sahoo & Bhattacharya, 2018) is currently the most widely used PWM strategy for a cascaded H-bridge-based inverter. It can be further divided into carrier cascaded PWM and carrier horizontal-phase-shift PWM. In this project, we use a bipolar horizontal-phase-shift PWM strategy wherein for N cascaded H-bridges, each triangular carrier that has a phase angle difference of $2\pi/N$ is compared with the same reference voltage signal to obtain the PWM pulse to drive the corresponding H-bridge. The output voltages that are of different phase angles then are superposed to form the compensation voltage of the DVR.

C. *Virtual impendence control strategy*

Feed-forward control, feedback control and composite control (Le, Li, Zhu, Zhang, & Li, 2018) are commonly used linear control strategies for DVRs. In this paper, we adopt a dual-loop control scheme to address the resonance problem associated with the single-stage output LC filter and to improve the stability of the DVR system. This controller consists of an outer capacitor voltage feed-forward loop and an inner inductor current feedback loop, as shown in Figure 5.

In Figure 5, u_{ref} and u_{dvr} is the reference and output voltage of the DVR, respectively; u_{inv} and i_{inv} is respectively the output voltage and current of the inverter; i_s and i_c is the system current and the current in capacitor C_f, respectively, and $i_c = i_{inv}+i_s$. The PI controller has an expression of k_p+k_i/s; $k_{PWM}\in[0.8–1]$ is the attenuation coefficient of the DVR inverter; L_f and C_f is, respectively, the inductance and capacitance of the LC filter, and k is the current feedback coefficient.

The transfer function of the dual-loop control system can be derived from Figure 5 as:

$$u_{dvr} = \frac{(K_{PWM}(K_P+1))s + K_{PWM}K_i)u_{ref} - L_f s^2 i_s}{L_f C_f s^3 + k\cdot K_{PWM}C_f s^2 + (K_{PWM}K_P+1)s + K_{PWM}K_i} \tag{5}$$

As aforementioned, a large fault current following a downstream short-circuited fault also can decrease the bus voltage u_s. Responding to this voltage sag may cause a current that is larger than

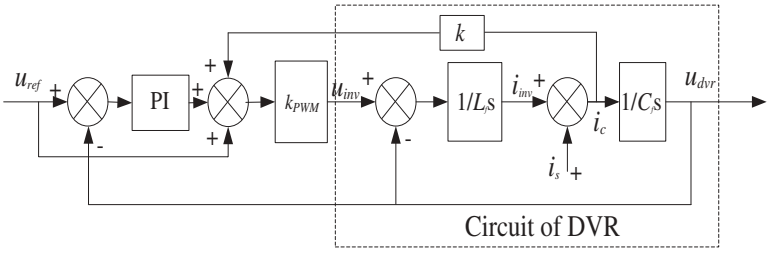


Figure 5. Dual-loop control of the DVR.

the fault current before compensation to flow through the DVR, thus damaging the DVR system. In this project, we control the DVR to serve as a fault current limiter instead of operating the DVR in a bypass status, with the aims to recover the bus voltage from a sag by limiting the fault current.

Controlling a DVR to behave as a resistor R_0 in series with an inductor L_0 implies:

$$u_{ref} = (R_0 + sL_0)i_s \tag{6}$$

Eliminating variable u_{ref} by substituting formula (6) into (5) leads to:

$$\frac{u_{dvr}}{i_s} = \frac{g_2 s^2 + g_1 s + g_0}{a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{7}$$

where: $g_2 = k_{PWM}(k_p + 1)L_0 - L_f$, $g_1 = k_{PWM}(k_i L_0 + (k_p + 1)R_0)L_0$, $g_0 = k_{PWM}k_i R_0$, $a_3 = L_f C_f$ $a_3 = k_{PWM}kC_f$, $a_1 = k_{PWM}k_P + 1$,$a_0 = k_{PWM}k_i$.

In recent years, series capacitance compensation technology has been gradually applied in distribution networks to solve the increasingly prominent low-voltage problem. A practical application of this technology in a 66-kV distribution network has been reported in (Ren, Yang, Xie, Wang, & Feng, 2011). Similarly, to control a DVR to operate as a resistor R_0 in series with a capacitor C_0, the relationship between u_{ref} and i_s can be expressed as:

$$u_{ref} = (R_0 + 1/(sC_0))i_s \tag{8}$$

Eliminating variable u_{ref} by substituting formula (8) into (5) leads to:

$$\frac{u_{dvr}}{i_s} = \frac{h_3 s^3 + h_2 s^2 + h_1 s + h_0}{(a_3 s^3 + a_2 s^2 + a_1 s + a_0)s} \tag{9}$$

where $h_3 = -L_f$, $h_2 = k_{PWM}(k_p + 1)R_0$, $h_1 = k_{PWM}(k_i R_0 C_0 + k_p + 1)/C_0$, $h_0 = k_{PWM}k_i/C_0$.

Besides the benefit of solving the low-voltage problem of a distribution network in a cost-effective way, the complex bypass circuit of a DVR operating as a series compensation device can be totally removed, thus improving the reliability and reducing the investment of a DVR.

Figure 6 shows the frequency response characteristics of formula (7) with L_0 = 3 mH and R_0 = 1 Ω and that of formula (9) with C_0 = 600 μF and R_0 = 3 Ω.

Figure 6 shows that in the frequency range below 100-Hz, both amplitude and phase frequency response of the DVR agree well with those of a real series *RL* or *RC* circuit, verifying that our virtual impedance control strategy is very effective in controlling a DVR to behave as a virtual impedance with arbitrary values. In practice, it is more reasonable for a DVR to operate as a pure inductor or a capacitor since that a resistor always implies an active power exchange between DVR and external power system.

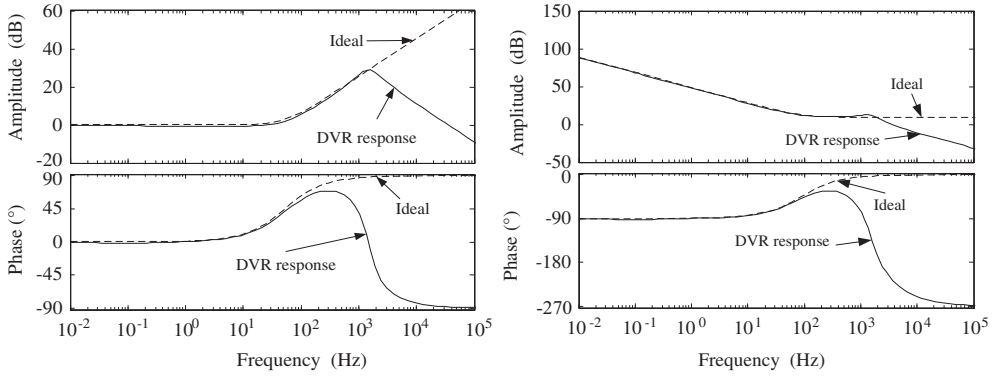


Figure 6. Frequency response of a DVR using virtual impedance control strategy.

V. Simulation verification

Figure 7 is the single-line diagram of a 10-kV bus of the 110-kV substation where our regional compensation DVR is to be installed to protect the sensitive loads in feeder lines F7 and F17, the total equivalent impedance of these two feeder lines is 0.119+ j0.127-Ω. The total capacity of the loads to be protected is about 15-MVA with a lagging power factor of 0.95. The simulation model of the whole system has been built using PSCAD software.

A. *Voltage sag compensation*

Assuming an LLG (phases A and C) fault occurs at point F in feeder line F11 at t= 0.5-s. The simulation results are illustrated in Figure 8.

It can be seen from Figure 8(a) that before the clearance of the short-circuited fault, phases A and C voltage drops from 8.29-kV to 4.51-kV and 3.82-kV, respectively, and phase B voltage swells from 8.29-kV to about 12-kV. By comparing Figure 8(b,c), we can learn that the symmetry degree of the three compensated load-side phase-to-neutral voltages has been effectively increased by using our zero-sequence voltage optimisation method, thus maximising the compensation ability utilisation of the DVR. As shown in Figure 8(d), the load-side phase-to-phase voltages recover to their rated values with a time-delay that is less than 5 ms. This result verifies that the regional compensation DVR has satisfying performances in terms of response speed and compensation accuracy.

B. *Fault current limitation*

In this simulation, a three-phase short-circuited fault is set downstream the DVR at t= 0.5 s with a duration of 0.2-s. The DVR is controlled as an FCL with L_0 = 100 mH. The simulation results are shown in Figure 9.

It can be seen from Figure 9(a,c) that when the DVR stands aside for a downstream fault, the system-side voltages drop to 40% of their rated values and the phase fault current is of a peak value of about 60-kA. Therefore, sensitive loads on other feeders that share the same bus as feeders F7 and F17 may be involved in a serious voltage sag. We can see from Figure 9(b,d) that with the aid of an FCL function provided virtually by the DVR, the fault current is limited significantly and the system voltages are restored to normal levels after a very short transient process. These results

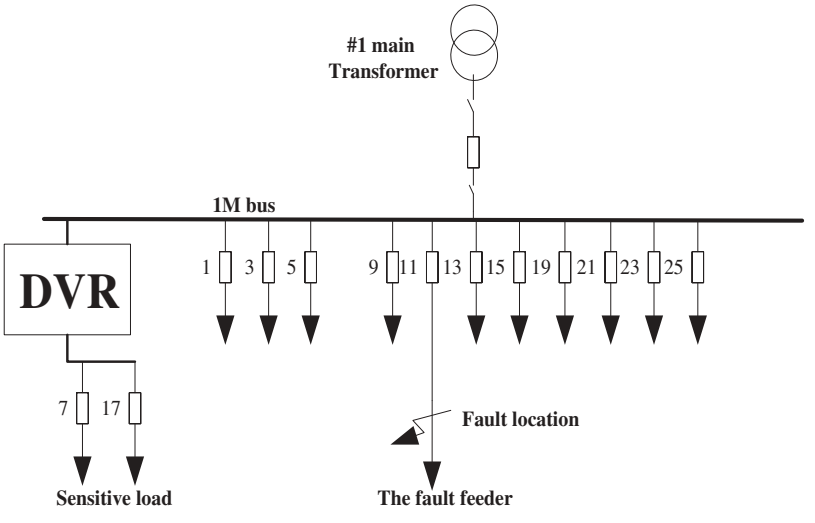
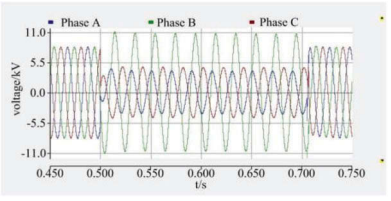
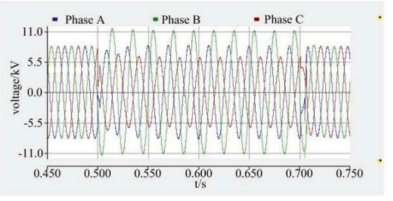


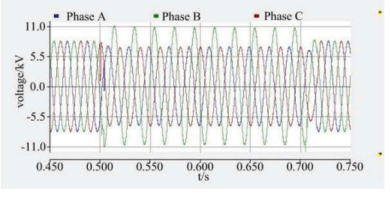
Figure 7. Single-line diagram of a 10-kV bus and its feeders.



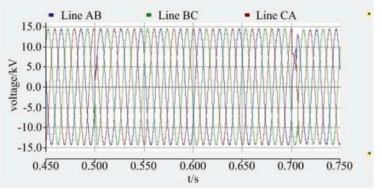
(a) system-side phase-to-neutral voltages



(b) load side phase-to-neutral voltages without zero-sequence component optimization

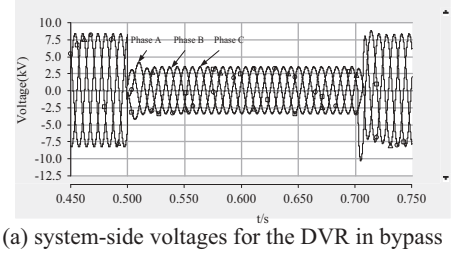


(c) load-side phase-to-neutral voltages with zero-sequence component optimization

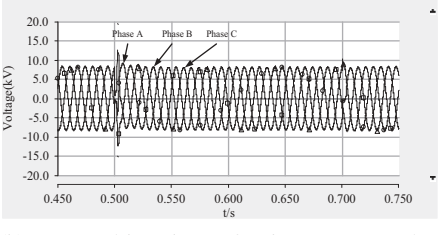


(d) load-side phase-to-phase voltages

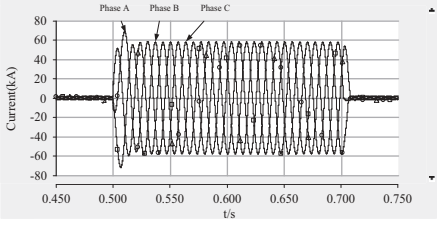
Figure 8. Simulation results for an LLG fault.



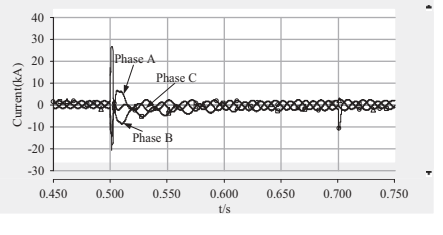
(a) system-side voltages for the DVR in bypass operation



(b) system-side voltages for the DVR operating as an FCL



(c) System currents for the DVR in bypass operation



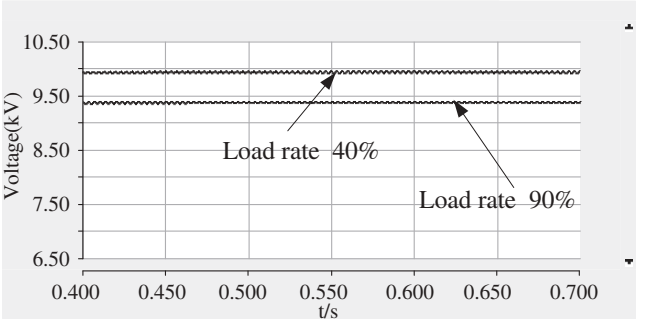
(d) System currents for the DVR operating as an FCL

Figure 9. Simulation results of the FCL function of the DVR.

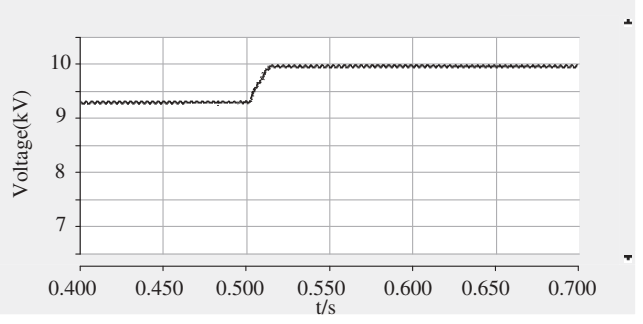
verify the effectiveness of our virtual impendence control strategy in controlling the DVR to operate as an FCL.

C. *Low-voltage compensation*

Figure 10 shows the RMS values of the load-side voltages for the DVR operating in SC mode.



(a) DVR in bypass operation



(b) DVR operating as an SC

Figure 10. Load voltages under different operation modes of the DVR.

Figure10(a) informs us that if the DVR is in hot standby mode under normal operation of the power system, the RMS value of load voltage drops from 10.0-kV to about 9.4-kV with the load rate increasing from 40% to 90%, namely, a −6% voltage deviation. While when controlling the DVR as an SC with C_0 = 10 mF at t = 0.5 s, we can see from Figure 10(b) that the load voltage recovers to its normal value of about 9.9-kV. This result verifies the effectiveness of the SC function of the DVR in tackling low-voltage problem.

VI. Field experimental results

A 10-kV 5-MW regional compensation DVR has been developed and installed in a 110-kV substation of Shenzhen power grid. This DVR is structured by a three-phase independently controlled inverter, and each phase is composed of six cascaded H-bridges with independent DC energy supply. Each H-bridge is characterised by four 1700-V/1200-A IGBTs and a 1000-V DC voltage. Figure 11 shows the appearance and internal arrangement of this device. All cabinets, which include the ring network cabinet, isolation starting cabinet, electronic and mechanical bypass cabinet, inverter cabinet and control cabinet, are integrated into a container.

A. *High-power experiment of the inverter*

Figure 12 shows the results of high-power experiment of a single-phase inverter burdened with a resistance-inductance load with a power factor of 0.9 lagging.

As observed in Figure 12, the inverter current raises sharply to 440-A with an output voltage of 2.34-kV, which basically satisfies the proposed performance index for the inverter listed in Table2.

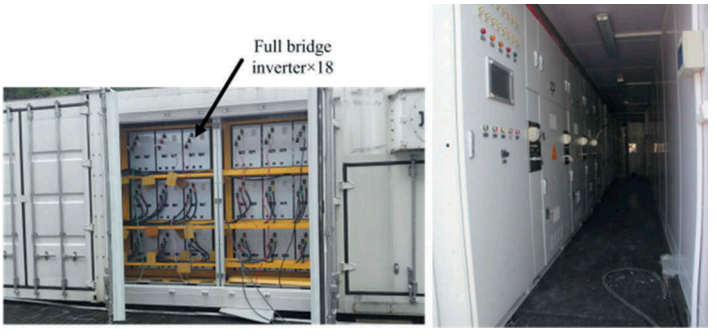


Figure 11. Appearance and internal arrangement of the DVR.

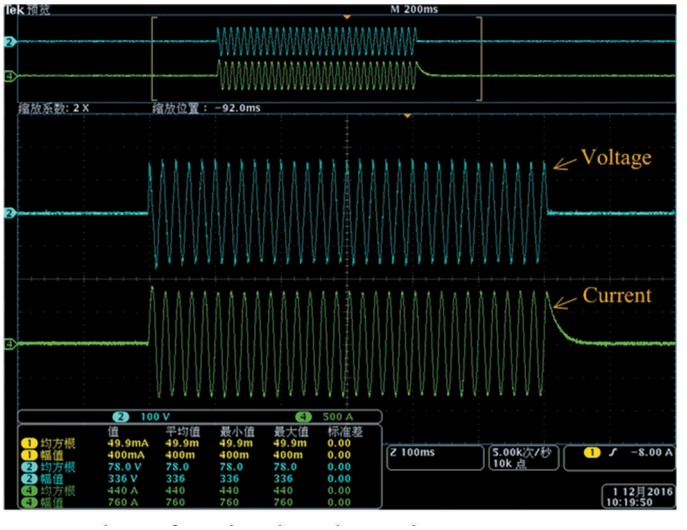


Figure 12. High-power test results of a single-phase inverter.

B. *Voltage sag compensation experiment*

We conduct several experiments to test the compensation performance of the DVR. Short-circuited faults are produced by a self-developed fault generator. Figure 13 illustrates the phase-A voltage during a systematic three-phase fault on the system side of the DVR with a sag degree of 50%.

Figure 13 shows that the system phase A voltage decreases from 5.95-kV to about 3-kV (i.e. a 50% voltage sag) after the occurrence of the fault, whereas the load voltage remains at basically 5.95 kV during the fault process, and the response time is less than 5 ms. These results verify that the developed DVR can effectively compensate voltage sags and satisfy the proposed performance indicators.

C. *Virtual impedance control experiment*

These experiments are performed on a scaled prototype DVR with a rated voltage of 380-V instead of on the 10-kV device. The load is constructed by two series 38.7-Ω resistor with a rated power of 2500-W, and short-circuited fault is produced by grounding three parallel power resistors. Figure 14 shows the system current in a downstream fault when the DVR is controlled as a 150-mH virtual inductor.

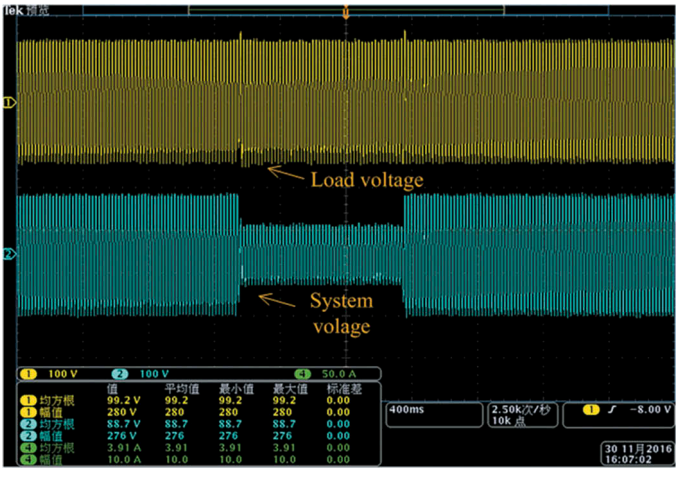
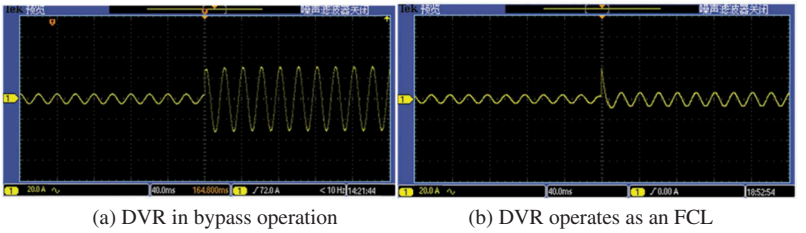


Figure 13. Voltage sag compensation experiment results.



(a) DVR in bypass operation (b) DVR operates as an FCL

Figure 14. System current in a downstream fault.

Figure 14 shows that the pre-fault system current is nearly 4.8-A and reaches 28.2-A during the downstream fault for the bypass operation of the DVR. When the DVR acts as an FCL, the fault current can be limited to 7.2-A. These results prove that the DVR successfully takes the role of an FCL with the help of our virtual impendence control strategy.

Figure 15 shows the load voltage when the DVR is controlled as an SC with a 450-uF virtual capacitor. A 10-mH inductance is inserted into the line to simulate the line impedance, and the load is four paralleling 38.7-Ω resistors.

As seen from Figure 15, when the DVR operates in a bypass mode, the load voltage decreases to nearly 290-V because of the voltage loss in the 10-mH inductor, whereas it increases to 350-V after

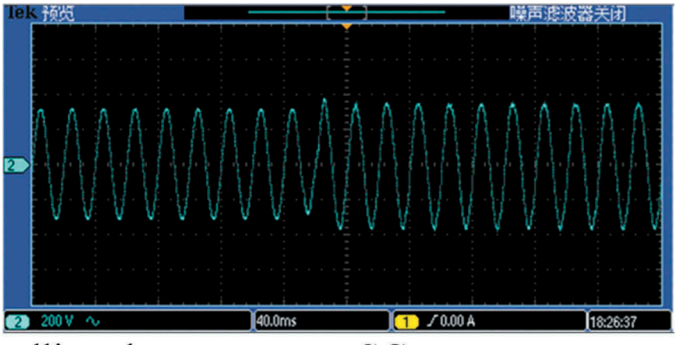


Figure 15. Results of controlling the DVR as an SC.

the DVR is controlled as an SC. These results prove that the DVR also can take the role of an SC with the help of our virtual impendence control strategy.

VII. Conclusions

The middle-voltage regional compensation dynamic voltage restorer offers a new cost-effective way to improve the power quality of power systems. A 10-kV/5-MW DVR has been installed in a 110-kV substation in Shenzhen power grid in December 2016, which is the first high-power MV regional power quality management demonstration project in China. Simulation and experimental results prove that this device can simultaneously protect plenty of sensitive loads from voltage sags, and under the control of our virtual impedance strategy, the DVR can function as a fault current limiter or a series compensator, which can improve the technical and economic performance of this device further.

Disclosure statement

No potential conflict of interest was reported by the authors.

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